Table 2.26: Device Library and Device Description

### RESISTOR

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### CAPACITOR

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### EC HISTORY

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**Note:**
- Tolerance specifications are shown in parentheses: (J: 5%, F: 1%, D: 0.5%, B: 0.1 %).
- Symbol name format: S<value><value><value><size><tolerance>.
- Symbol name format for resistors: R<value><size><tolerance>.
- Symbol name format for capacitors: C<value><size><tolerance>.
- **SC**: SMT Ceramic.
- **TC**: POS cap or SP cap.
- **D1U**: 0.1uF.
- **10V**: Voltage rating.
- **M**: Tolerance M, K, Z
- **X7R/X5R**: Y5V
- **-1**: Symbol version, non-EE characteristic.

**CAUTION:**
- Planar ID and Planar PCB Version are not relevant to this document.
need a Via to measure VCCIO_SEL voltage level.

no 0.01 ohm 1% 0402 RES
DEBUG Interface for Processor.

**XDP1**

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**FVT Logic**

DEBUG Interface for PCH.

**XDP2**

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**FVT Logic**

---

**Title**: XDP Connector

**Size**: A3

**Document Number**: 11 101

**Date**: Friday, March 09, 2012

**Rev**: 1

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GND GUARDING
EACH SIGNAL WIDTH DEPENDS ON ZO (TRACE IMPEDANCE)
SPACING = 20MIL

EACH SIGNAL WIDTH DEPENDS ON ZO (TRACE IMPEDANCE)
SPACING = 20MIL
System DP Connector

Docking DP Connector A

Docking DP Connector B

Placement Near Docking Connector

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Date: Sheet 38 Friday, March 02, 2012

Dash-2
C420 AND 0 OHM RESISTOR SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE

HIGH VOLTAGE 1500PF CAP IS OPTIONAL

PATTERN MUST BE SHORT AND WIDE

ESD REASON
Place close to EC

Width = 6 mil & Spacing = 10 mil for three Output traces

Layout Comment:
(1) Avoid routing under DCDC switching area.
After SDV

ST19NP18ER28PVMO (71.19N18.T0W)

ST33ZP24AR28PVxx
xx="OG" for SDV(71.03324.A0W),
"RC" for FVT, PreSIT (FW 1.2.C.0)(71.03324.C0W)
SC for SIT (not PreSIT) FW 1.2.D.0(71.03324.D0W)
These pins are used for VCC3SW force off.

PTC Placement List

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Input cap: 10μF 10% 25V 4pcs. These MLCCs must be placed symmetrically on Top and Bottom.

Keep these two signals as a pair routing!!

Please R1316 and C842 near EC
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RF decoupling caps
named as RFCxxx

Long power trace EMI decoupling caps
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**Duplicity**

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**Battery Authentication**

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--- External EEPROM | Y | Y | Y | N |